PRINT OF DRAWINGS
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UTILITY PATENT APPLICATION TRANSMITTAL
(Large Entity)

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Docket No.
BU9-99-175
Total Pages in this Submission
3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 U.S.C. 111(a) and 37 C.F.R. 1.53(b) is a new utility patent application for an invention entitled:

COPPER PAD STRUCTURE

and invented by:

Wayne J. Howell
Ronald L. Mendelson
William T. Motsiff

jc678 U.S. PTO 09/526394 03/16/00

If a CONTINUATION APPLICATION, *check appropriate box and supply the requisite information:*

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

☐ **Continuation** ☐ **Divisional** ☐ **Continuation-in-part (CIP)** of prior application No.: _____

Which is a:

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Enclosed are:

Application Elements

1. ☒ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **16** pages and including the following:

   a. ☒ Descriptive Title of the Invention

   b. ☐ Cross References to Related Applications *(if applicable)*

   c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*

   d. ☐ Reference to Microfiche Appendix *(if applicable)*

   e. ☒ Background of the Invention

   f. ☒ Brief Summary of the Invention

   g. ☒ Brief Description of the Drawings *(if drawings filed)*

   h. ☒ Detailed Description

   i. ☒ Claim(s) as Classified Below

   j. ☒ Abstract of the Disclosure

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Application Elements (Continued)

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   a. ☒ Formal Number of Sheets 2
   b. ☐ Informal Number of Sheets

4. ☒ Oath or Declaration
   a. ☒ Newly executed *(original or copy)* ☐ Unexecuted
   b. ☐ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   c. ☒ With Power of Attorney ☐ Without Power of Attorney
   d. ☐ *DELETION OF INVENTOR(S)*
   Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. 1.63(d)(2) and 1.33(b).

5. ☐ Incorporation By Reference *(usable if Box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche *(Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy *(identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☒ Assignment Papers *(cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☒ Copies of IDS Citations

12. ☐ Preliminary Amendment

13. ☒ Acknowledgment postcard

14. ☒ Certificate of Mailing
   ☐ First Class ☒ Express Mail *(Specify Label No.):* EL046032795US

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Accompanying Application Parts (Continued)

15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*

16. ☐ Additional Enclosures *(please identify below):*

Fee Calculation and Transmittal

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	21	- 20 =	1	x $18.00	$18.00
Indep. Claims	3	- 3 =	0	x $78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐					$0.00
				BASIC FEE	$690.00
OTHER FEE *(specify purpose)* _____					$0.00
				TOTAL FILING FEE	$708.00

☐ A check in the amount of to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of **$708.00** as filing fee.
- ☒ Credit any overpayment.
- ☒ Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
- ☐ Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Signature

Dated: 3/16/00

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EXPRESS MAIL EL046032795US

APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAMES: Wayne J. Howell
Ronald L. Mendelson
William T. Motsiff

TITLE: COPPER PAD STRUCTURE

DOCKET NO.: BU9-99-175

INTERNATIONAL BUSINESS MACHINES CORPORATION

COPPER PAD STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to semiconductor integrated circuits and more particularly to the pads and solder balls used to make electrical connections between the integrated circuit devices having copper wiring and the external electrical environment.

Description of the Related Art

Once the manufacturing processes for the last wiring layer of an integrated circuit die is completed, additional processing is required to form connections between the die and its associated printed circuit card or board. This additional processing allows connection to the external electrical environment and is sometimes referred to as "back end of line" or BEOL processing.

One aspect of BEOL processing can involve the formation of lead/tin solder balls, e.g. C4 connections, on the exterior of the integrated circuit die. The solder balls are used to make electrical connection to the last layer of wiring and

underlying circuitry contained on the integrated circuit device. In a later assembly process, the free surface of the solder ball is joined to corresponding wiring pads on a printed circuit card, flex circuit cable or ceramic die carrier. Figure 1 illustrates a cross section of a conventionally fabricated integrated circuit device having aluminum wiring and solder ball connections. More specifically, the exterior of the integrated circuit has a passivation layer 12, typically comprised of silicon dioxide, silicon nitride or silicon oxide/nitride combinations. The passivation layer 12 covers the aluminum last wiring layer 11 and the passivation layer 12 contains an opening (via hole) that exposes the surface of the last wiring layer. The passivation layer is not planar, but rather conformal to the underlying surface that contains the final wiring layer. The via hole is conventionally formed using a standard lithographic and etching process.

Typically, a pad 13 (e.g., liner/barrier) is formed over the via hole. The pad 13 forms a "transition metallurgy" that provides a robust mechanical connection between the solder ball 14 and both the wiring layer 11 and the passivation layer 12. The pad 13 also provides low and stable electrical (contact) resistance between the solder ball 14 and the last wiring layer 11. The pad 13 is typically comprised, for example, of one or more of chromium, tungsten or titanium with overlayers of solderable metals such as copper or gold. Conventionally, the chromium, tungsten, etc. of the pad 13 are placed in contact with the aluminum wiring layer 11 and the solderable metal(s) of the pad 13 is

placed in contact with the solder 14. During solder ball 14 formation on the integrated circuit and subsequent attachment of the solder balls 14 to a printed circuit card, the lead or tin in the solder 14 may completely react with the solderable metal and bring lead or tin into contact with the chromium, tungsten, etc. layer.

In the case of aluminum last wiring layers, there is limited inter-metallic formation between the aluminum 11 and lead and tin in the solder ball 14. Any tin that diffuses through micro cracks or grain boundaries of the pad 13 does not result in rapid, strong inter-metallic formation with aluminum. Also, with aluminum wiring, there is insufficient reaction to consume the pad 13, i.e. react it into inter-metallic, or propagate inter-metallic into the aluminum wiring line.

However, high performance integrated circuits have introduced copper as the last wiring layer. Copper has lower electrical resistance than aluminum and, as a result, yields faster propagation of a signal through a wiring line, increasing the operational speed of the integrated circuit. Copper however, readily reacts with (forms inter-metallics with) the tin 14. The copper-tin inter-metallics have an associated volume change, that can be both mechanically weak and have increased electrical resistance. A mechanically weak inter-metallic can degrade the reliability, e.g. ability to withstand thermal cycles, of the integrated circuit device. The increased electrical resistance of the inter-metallic can also slow the

signal propagation both between the device and its external connection and more particularly through internal device wiring.

When sufficient excess of tin exists in the solder ball 14, as in the case of a solder ball made from eutectic solder (63% tin, 37% lead), inter-metallic formation can be extensive, extending well into the wiring lines degrading signal propagation and potentially damaging dielectric films adjacent to the wires, because of the volume change associated with inter-metallic formation. There is, therefore, a need for an easy to manufacture pad structure which provides mechanically and electrically robust interconnections between copper wiring and solder balls without introducing the possibility of tin or lead diffusion into the last copper wiring lines. The invention described below provides such a pad structure, in a planar configuration.

SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a structure and method for forming mechanically and electrically robust interconnections between integrated circuit copper wiring and solder balls, without possibility of tin or lead diffusion from the solder balls into the last copper wiring lines.

One embodiment of the invention comprises a metallurgical structure that includes a passivation layer, a via through the passivation layer extending to a

metal line within the metallurgical structure, a barrier layer lining the via, a metal plug in the via above the barrier layer, the metal plug and the metal line comprising a same material, and a solder bump formed on the metal plug.

The "same material" can be copper and the barrier layer can be one or more layers of Ti, TiN, Ta, and TaN. The barrier layer and the metal plug prevent elements within the solder bump from diffusing to the metal line. The metal plug, the barrier layer and the passivation layer form a planar exterior surface of the metallurgical structure. The solder ball can be in direct contact with the metal plug or the structure can include a second barrier layer above the metal plug and a second metal plug above the second barrier layer, where the second metal plug is in direct contact with the solder ball.

Another embodiment of the invention comprises a method of forming an integrated circuit structure that includes forming a via through an exterior of the integrated circuit structure to internal components of the integrated circuit structure, lining the via with a barrier layer, forming a plug above the barrier layer, the plug and the internal components comprising a same material, and forming a connector on the plug.

The "same material" can again comprises copper, and the barrier layer can comprise one or more layers of Ti, TiN, Ta, and TaN. Again, the barrier layer prevents elements within the connector from diffusing to the internal components.

The method also includes a process of polishing the integrated circuit structure such that the plug, the barrier layer and the exterior form a planar surface. The connector can be formed to be in direct contact with the plug or the inventive process can include forming a second barrier layer above the plug and forming a second plug above the second barrier layer, such that the second plug is in direct contact with the connector.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings, in which:

Figure 1 is a schematic diagram of a conventional via, pad, and solder ball;

Figure 2 is a schematic diagram of the inventive via, plug and solder ball; and

Figure 3 is a schematic diagram of another embodiment of the inventive via, plug and solder ball.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

As discussed above, conventional BEOL structures, such as that shown in Figure 1, suffer from the disadvantage that, when copper is used as the last metalization layer, tin diffusion can result in a structure that is not mechanically and electrically robust. The invention overcomes these problems by using a novel copper plug and barrier layer, as discussed below.

A first embodiment of the invention is shown in Figure 2. The invention replaces the conventional pad structure 13 as described above with the one shown in Figure 2. The last copper wiring layer 20 on the integrated circuit device is typically formed using a damascene process and is covered with an appropriate passivation films stack 21. The passivation films stack is typically comprised of one or more layers of silicon dioxide, silicon nitride or combinations thereof, deposited by chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), etc. methods. An opening (via hole) 22 is formed in the passivation films stack using conventional lithographic and etching techniques employing photoresist and reactive ion etching.

After removal of the photoresist, the stack of films 21 is sequentially blanket deposited with a liner 23 and then a copper plug 24. Initially, the "liner/barrier" film(s) 23 comprised of Ti, TiN, Ta, TaN, or combinations thereof is deposited by sputtering or reactive sputtering techniques. The total thickness of

the liner films stack 23 is between 100 and 1000A thick. The liner films 23 are not limited to those specified above, but as would be known by one ordinarily skilled in the art could be any substance that is selected to have the properties of good adhesion to both copper wiring and the overlayer passivation films, relatively low electrical resistance and excellent resistance to diffusion by lead, tin and copper.

Next, the copper plug 24 is deposited over the liner by sputtering, electroplating or evaporation techniques with sufficient thickness to be at least coplanar with the top of the passivation films 21. Chemical mechanical polishing (CMP) is then used to remove the copper 24 and the liner 23 from the field areas leaving a plug of liner 23 and copper 24 in the via hole. If the passivation films stack 21 was not initially planar, the CMP process can be continued (with the same or a different slurry) after the liner is removed to planarize both the passivation 21 and filled vias 22.

A lead/tin solder ball 25 is then formed on the via plug 24 using evaporation through a mask, solder ink jet or other well known techniques. The amount of inter-metallic formation is controlled by the amount of tin in the solder ball and the thickness of the copper 24 in the filled via 22 which in turn is controlled by the thickness of the passivation films 21 and the liner 23.

A second embodiment of the invention, shown in Figure 3, provides a redundant "liner/barrier" layer 35 in the filled via 22 to achieve minimum inter-

metallic formation and maximum protection of the integrated circuit copper wiring 20 from diffusion of elements contained in the solder ball. In this embodiment, the via 22 is filled as described in the first embodiment. The copper 24 in the filled via 22 is then selectively recessed using an aqueous solution of ammonium persulfate or other solution that will preferentially etch copper rather than the liner. Typically, the copper 24 is recessed between 1000 and 10000A to form a recessed copper plug 34 (e.g., copper plug 1). A second liner/barrier 35 comprised of Ti, TiN, Ta, TaN, or combinations thereof are blanket deposited over the recessed copper plug 34 by sputtering or reactive sputtering techniques. A second copper film 36 (e.g., copper plug 2) is deposited over the blanket liner/barrier film(s) by sputtering, electroplating or evaporation techniques with sufficient thickness to be at least coplanar with the top of the passivation films.

Again the liner/barrier 35 thickness is controlled to be less than the amount which would be coplanar with the top of the passivation films stack, insuring that a thin copper film 36 remains in the center of the via when the subsequent chemical, mechanical polish is complete. A lead / tin solder ball 37 is formed on the second via plug 36 using evaporation through a mask, solder ink jet or other well-known techniques.

Therefore, the invention replaces the conventional liner 13 with a copper plug 24, 34, 36 and barrier 23, 35. This structure produces a number of a advantages when compared to the conventional structure. For example, the

copper plug/liner of the invention prevents tin diffusion to the underlying copper wiring layer 20. The copper plug consumes any tin which would otherwise diffuse to the underlying copper wiring. The invention is not limited to copper wiring. Instead, the invention is applicable to any material with similar characteristics so long as the plug and the underlying wiring are of the same material. This allows the plug to consume the potential impurities before they reach the underlying wiring layer. The barrier layer acts to stop any tin impurities which are not consumed by the copper. Further, the invention is different than structures which utilize a thin copper layer in that the copper plug provides sufficient thickness to consume large amounts of tin impurities and to form a strong inter-metallic bond with the lead/tin solder ball.

Additionally, the invention produces a structure which is co-planer with the passivation layer 21, which makes the formation of the lead/tin solder ball 25, 37 simpler and less prone to manufacturing defect. Also, the physical strength of the copper plug/liner structure is superior to the conventional liner 13 (because copper makes a very strong bond with tin/lead solder balls) and, therefore, provides superior mechanical bonding strength between the integrated circuit and the solder ball 25, 37.

While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A metallurgical structure comprising:

a passivation layer;

a via through said passivation layer extending to a metal line within said metallurgical structure;

a barrier layer lining said via;

a metal plug in said via above said barrier layer, said metal plug and said metal line comprising a same material; and

a solder bump formed on said metal plug.

2. The metallurgical structure in claim 1, wherein said same material comprises copper.

3. The metallurgical structure in claim 1, wherein said barrier layer comprises one or more layers of Ti, TiN, Ta, and TaN.

4. The metallurgical structure in claim 1, wherein said barrier layer and said metal plug prevent elements within said solder bump from diffusing to said metal line.

5. The metallurgical structure in claim 1, wherein said metal plug, said barrier layer and said passivation layer form a planar exterior surface of said metallurgical structure.

6. The metallurgical structure in claim 1, wherein said solder ball is in direct contact with said metal plug.

7. The metallurgical structure in claim 1, further comprising a second barrier layer above said metal plug and a second metal plug above said second barrier layer, said second metal plug being in direct contact with said solder ball.

8. An integrated circuit structure comprising:

internal components within an exterior covering;

a via extending through said exterior covering to said internal components;

a barrier layer lining said via;

a plug in said via above said barrier layer, said plug and said internal components comprising a same material; and

a connector formed on said plug.

9. The integrated circuit structure in claim 8, wherein said same material comprises copper.

10. The integrated circuit structure in claim 8, wherein said barrier layer comprises one or more layers of Ti, TiN, Ta, and TaN.

11. The integrated circuit structure in claim 8, wherein said barrier layer and said plug prevent elements within said connector from diffusing to said components.

12. The integrated circuit structure in claim 8, said plug, said barrier layer and said exterior covering form a planar exterior surface of said integrated circuit structure.

13. The integrated circuit structure in claim 8, wherein said connector is in direct contact with said plug.

14. The integrated circuit structure in claim 8, further comprising a second barrier layer above said plug and a second plug above said second barrier layer, said second plug being in direct contact with said connector.

15. A method of forming an integrated circuit structure comprising:

forming a via through an exterior of said integrated circuit structure to internal components of said integrated circuit structure;

lining said via with a barrier layer;

forming a plug above said barrier layer, said plug and said internal components comprising a same material; and

forming a connector on said plug.

16. The method in claim 15, wherein said same material comprises copper.

17. The method in claim 15, wherein said barrier layer comprises one or more layers of Ti, TiN, Ta, and TaN.

18. The method in claim 15, wherein said barrier layer prevents elements within said connector from diffusing to said internal components.

19. The method in claim 15, further comprising polishing said integrated circuit structure such that said plug, said barrier layer and said exterior form a planar surface.

20. The method in claim 15, wherein said connector is formed to be in direct contact with said plug.

21. The method in claim 15, further comprising forming a second barrier layer above said plug and forming a second plug above said second barrier layer, such that said second plug is in direct contact with said connector.

COPPER PAD STRUCTURE

ABSTRACT

A structure (and method) for a metallurgical structure includes a passivation layer, a via through the passivation layer extending to a metal line within the metallurgical structure, a barrier layer lining the via, a metal plug in the via above the barrier layer, the metal plug and the metal line comprising a same material, and a solder bump formed on the metal plug.

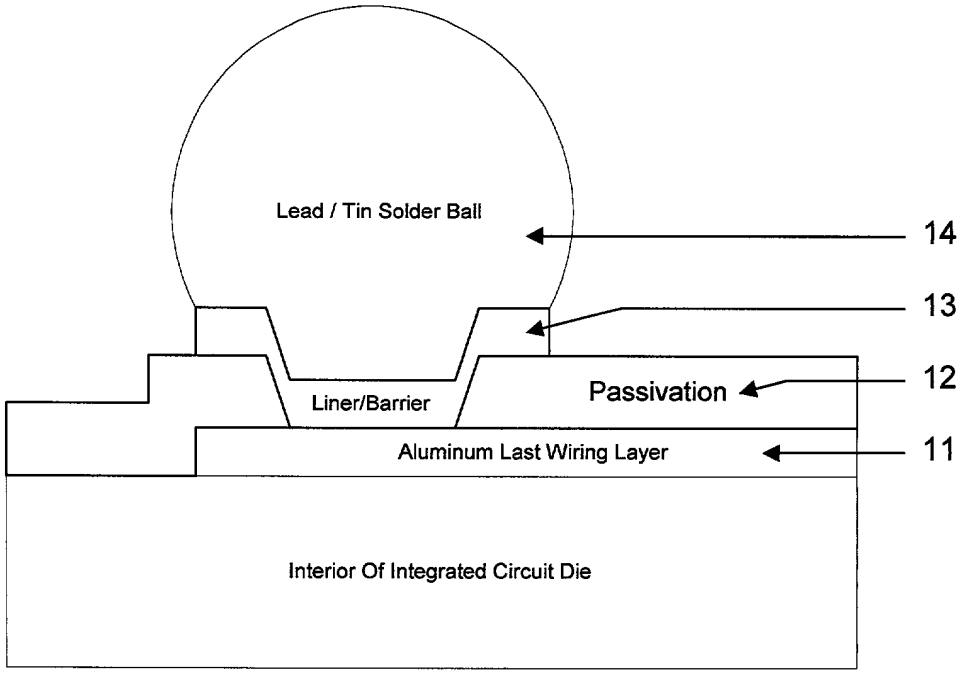

Figure 1

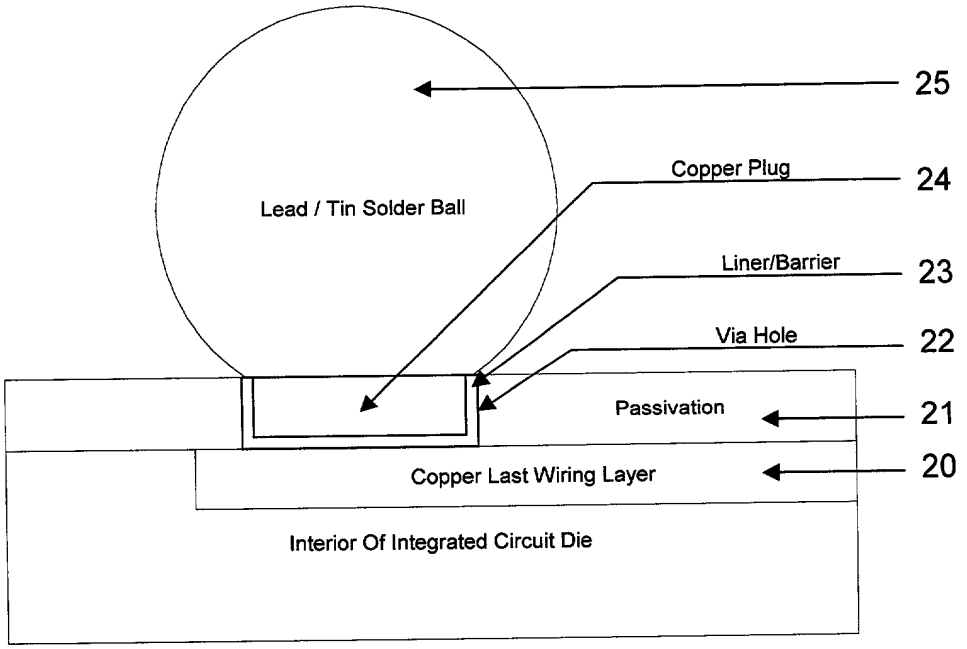

Figure 2

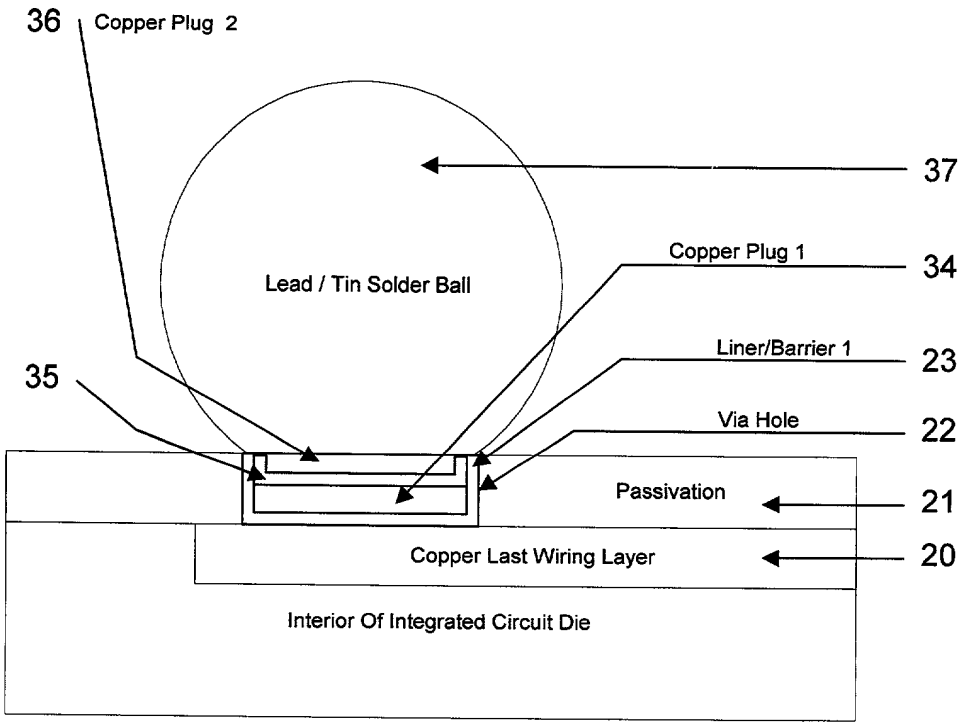
36
Copper Plug 2
37
Lead / Tin Solder Ball
Copper Plug 1
34
Liner/Barrier 1
23
35
Via Hole
22
Passivation
21
Copper Last Wiring Layer
20
Interior Of Integrated Circuit Die

Figure 3

IBM Docket No.: BU9-99-175

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **COPPER PAD STRUCTURE**

the specification of which:
(check one)

☒ is attached hereto.
☐ was filed on _____, as Application Serial No. _____ and was amended on _____.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):

Number	Country	Day/Month/Year	Priority Claimed

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S. Applications:

Serial No.	Filing Date	Status

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Tide 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: Mark F. Chadurjian (Reg. No. 30,739), Richard M. Kotulak (Reg. No. 27,712), James M. Leas (Reg. No. 34,372), William D. Sabo (Reg. No. 27,465), Eugene I. Shkurko (Reg. No. 36,678), Robert A. Walsh (Reg. No. 26,516), Howard J. Walter, Jr. (Reg. No. 24,832), Christopher A. Hughes (Reg. No. 26,914), Edward A. Pennington (Reg. No. 32,588), John E. Hoel (Reg. No. 26,279), Joseph C. Redmond, Jr. (Reg. No. 18,753), Richard A. Henkler (Reg. No. 39,220), Sean M. McGinn (Reg. No. 34, 386), and Frederick W. Gibb, III (Reg. No. 37,629).

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